What is Claimed:

1. A method of fabricating a semiconductor chip including a top passivation layer formed over the chip comprising the step of:

forming at least two alignment marks in or on the passivation layer.

2. The method according to claim 1 further comprising the step of selectively processing a portion of the chip using the marks to locate said portion, the processing selected from etching and adding material.

3. The method according to claim 1 wherein the alignment marks comprise a metal formed on a top surface of the passivation layer.

4. The method according to claim 1 wherein the chip includes an additional underlying passivation layer, and the alignment marks are formed by depositing material over the underlying passivation layer, and then covering with the top passivation layer.

5. The method according to claim 1 wherein the alignment marks comprise etched areas formed in the top surface of the top passivation layer.

6. The method according to claim 1 wherein the marks are in the shape of crosses.

7. The method according to claim 6 wherein the marks include rectangular portions at one or more ends of the crosses, the number of portions depending upon the quadrant of the chip in which the mark is positioned.

8. The method according to claim 1 wherein there are at least four alignment marks, one at each corner of the chip.

9. A semiconductor chip comprising:

a passivation layer as a top layer; and

at least two alignment marks formed in or on the passivation layer to provide topological features for locating selected areas of the chip.

10. The chip according to claim 9 wherein the alignment marks comprise a metal formed on a top surface of the passivation layer.

11. The chip according to claim 9 wherein the chip includes an additional underlying passivation layer, and the alignment marks are formed by material formed over the underlying passivation layer and covered by the top passivation layer.

12. The chip according to claim 9 wherein the alignment marks comprise etched areas formed in the top surface of the top passivation layer.

13. The chip according to claim 9 wherein the marks are in the shape of crosses.

14. The chip according to claim 13 wherein the marks include rectangular portions at one or more ends of the crosses, the number of portions depending upon the quadrant of the chip in which the mark is positioned.

15. The chip according to claim 9 wherein there are at least four alignment marks, one at each corner of the chip.